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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/579,239	05/12/2006	Koichiro Tanaka	0756-7682	1310

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EXAMINER	
SMITH, BRADLEY	
ART UNIT	PAPER NUMBER
2894	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/579,239	TANAKA ET AL.	
	Examiner	Art Unit	
	Bradley K. Smith	2894	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 July 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6,7 and 11-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6,7 and 11-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3, 4, 6, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu (US 6,559,015) in view of Semiconductor Energy Lab (JP 2001-308344),Yamazaki (US 20030085720) and Sugioka et al. (WO 03/099508 published 4/12/03 (parent of US 2006/0091122 which is used as a an English translation)). Yu disclose forming a gate insulating film (202) over a semiconductor layer of a silicon substrate; forming a gate electrode over the gate insulating film (208); selectively injecting impurities into the semiconductor layer to form an impurity region (fig. 8). Regarding claim 3, Yu disclose the second impurity region (258, 260) is a source drain region (contact junctions) [col. 7 lines 31-40]. Regarding claim 4, Yu disclose the impurity region is an extension region (252,254) of the transistor [col. 6 lines 55-67].

Yu fails to disclose processing a laser beam having a fundamental wave into a long beam on a surface of the impurity region, the moving the surface of the impurity region relative to long beam to scan the laser beam to activate the impurity region and the laser beam having a pulse width of 1 femtosecond to 10 picoseconds.

However Semiconductor Energy Lab disclose processing a laser beam having a fundamental wave (claim 8 of Semiconductor Energy Lab).Regarding claims 6 and 13 Semiconductor Energy Lab disclose an Nd:YAG laser with a wavelength of 1064 nm (claim 8).

Yamazaki disclose processing of laser (wave) into a long beam on a surface of the impurity region (fig. 2), the moving the surface of the impurity region relative to long beam to scan the laser beam for annealing a semiconductor substrate[0065] (see figure 1, 7A, 11A-12C). Sugoika et al disclose using a femtosecond laser (abstract)

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Yu, Semiconductor Energy Lab, Yamazaki, and Sugoika because moving the surface of the impurity region and using a fundamental wave laser would be well within the ordinary skill in the art and would have yielded predictable results such as being able to move the substrate underneath the laser, and using a laser to anneal the substrate. Furthermore the femtosecond laser can generate multiphoton absorption [0094- from the child application] and using the fundamental wave laser would eliminate the need for non-linear optics.

Claims 2-4, 6, 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu (US 6,559,015) in view of Wang et al (US2003/0227056), Semiconductor Energy Lab (JP 2001-308344),Yamazaki (US 20030085720) and Sugioka et al. (WO 03/099508 published 4/12/03 (parent of US 2006/0091122 which is used as a an English translation)). Yu disclose forming a gate insulating film (202) over a semiconductor layer of a silicon substrate; forming a gate electrode over the gate insulating film (208); selectively injecting impurities into the semiconductor layer to form an impurity region (fig. 8). Regarding claim 3, Yu disclose the second impurity region (258, 260) is a source drain region (contact junctions) [col. 7 lines 31-

40]. Regarding claim 4, Yu disclose the impurity region is an extension region (252,254) of the transistor [col. 6 lines 55-67]. Regarding claim I5, Yu disclose 0.5-0.8 J/cm^2.

Yu fails to disclose a SOI substrate, processing a laser beam having a fundamental wave into a long beam on a surface of the impurity region, the moving the surface of the impurity region relative to long beam to scan the laser beam to activate the impurity region and the laser beam having a pulse width of 1 femtosecond to 10 picoseconds.

However Wang et al. disclose a semiconductor substrate SOI MOSFET [abstract]. Semiconductor Energy Lab disclose processing a laser beam having a fundamental wave (claim 8) and regarding claims 6 and 14 Semiconductor Energy Lab disclose a Nd:YAG laser with a wavelength of 1064 nm (claim 8). Yamazaki disclose processing of laser (wave) into a long beam on a surface of the impurity region (fig. 2), the moving the surface of the impurity region relative to long beam to scan the laser beam for annealing a semiconductor substrate[0065] (see figure 1, 7A, 11A-12C). Sugoika et al disclose using a femtosecond laser (abstract)

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Yu, Wang Semiconductor Energy Lab Yamazaki, and Sugoika because moving the surface of the impurity region and using a fundamental wave laser would be well within the skill in the art and would have yielded predictable results such as being able to move the substrate underneath the laser, and using a laser would anneal the substrate. Furthermore the femtosecond laser can generate multiphoton absorption [0094- from the child application], using the fundamental wave laser would eliminate the need for non-linear optics, and the SOI would reduce parasitic capacitance [Wang 0005].

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yu in view of Semiconductor Energy Lab (JP 2001-308344) Yamazaki (US 20030085720) and Sugioka et al. (US 2006/0091122) as applied to claims 1 above. Yu, Semiconductor Energy Lab, Yamazaki and Sugioka et al. disclose the claimed invention except for the laser beam is a pulsed laser light with a repetition rate of 10MHz or more. It would have been obvious to one of ordinary skill in the art at the time the invention was made to pulse the laser light with a repetition rate of 10MHz or more, since in has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In Re Aller, 105 USPQ 233. Furthermore, the higher repetition rate could enable one to process wafers faster.

Claims 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yu in view of Semiconductor Energy Lab (JP 2001-308344) Yamazaki (US 20030085720) and Sugioka et al. (US 2006/0091122) as applied to claim 1 above. Yu, Semiconductor Energy Lab, Yamazaki and Sugioka et al. disclose the claimed invention except for peak output power of the laser beam is $1GW/cm^2$ to $1TW/cm^2$. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have a peak output power of the laser beam at $1GW/cm^2$ to $1TW/cm^2$, since in has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In Re Aller, 105 USPQ 233. Furthermore, the higher peak power could enable one to process wafers faster (by doing more work per unit time).

Claims 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yu in view of Wang et al, Semiconductor Energy Lab (JP 2001-308344) Yamazaki (US 20030085720) and

Sugioka et al. (US 2006/0091122) as applied to claim 2 above. Yu, Semiconductor Energy Lab, Yamazaki and Sugioka et al. disclose the claimed invention except for peak output power of the laser beam is $1GW/cm^2$ to $1TW/cm^2$. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have a peak output power of the laser beam at $1GW/cm^2$ to $1TW/cm^2$, since in has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In Re Aller, 105 USPQ 233. Furthermore, the higher peak power could enable one to process wafers faster (by doing more work per unit time).

Response to Arguments

Applicant's arguments with respect to claims 1-4, 6, 7, 11-14 have been considered but are moot in view of the new ground(s) of rejection.

Furthermore the applicant has not provided evidence that one would understand "near infrared". The applicant contends that the terms are widely used in literature and can be readily understood, but the applicant has failed to provide any of this as evidence. Therefore the examiner understands that the 1064nm fundamental wavelength of the Nd:Yag laser is in the near infra red region.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bradley K. Smith whose telephone number is 571-272-1884. The examiner can normally be reached on 10-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Nguyen can be reached on 571-272-2402. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Bradley K Smith/
Primary Examiner, Art Unit 2894